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Reg. No. : .....

Name : .....

Third Semester B.Tech. Degree Examination, November 2014
(2013 Scheme)
13.304 : ANALOG ELECTRONICS (E)

Time : 3 Hours Max. Marks : 100

PART – A

Answer **all** questions briefly. **Each** question carries **2** marks.

1. What are the drawbacks of collector feedback bias circuit ?
2. Draw the labelled h-parameter equivalent circuit of CE configuration transistor.
3. What is base spreading resistance ? Why it is not considered at low frequencies ?
4. Sketch the cross-section of JFET, indicating the channel and depletion regions at
   i) pinch-off and
   ii) saturation
5. Why E-MOSFET is also called 'normally-off' MOSFET ?
6. Take two identically designed amplifiers for $A_V = 50$, $f_L = 50$ Hz cascade them. What will be the lower cut-off frequency of the cascaded combination ?
7. Derive equations to show that the gain stability of an amplifier is increased with the use of negative feedback.
8. Draw the electrical equivalent circuit for a crystal and explain its parameters.
9. Define slew rate. Explain its causes.
10. Draw the circuit of a voltage follower and state its properties.

(10×2= 20 Marks)

P.T.O.

PART – B

Answer **any one** full question from **each** Module. **Each** full question carries **20** marks

Module – I

11. a) Design a potential divider bias circuit diagram to have its Q-point at (6V, 2mA) using silicon transistor. The circuit is expected to have $S \leq 10$. **8**

    b) Derive the expressions for the S_V, S_I and S_β of the above circuit. **12**

OR

12. a) The h-parameters of a transistor are given as $h_{ie} = 2k$, $h_{re} = 2 \times 10^{-4}$, $h_{fe} = 80$, $h_{oe} = 50\,\mu$ A/V. Determine the current gain, voltage gain, input resistance and output resistance of the CE amplifier, if the load resistance is 10K and source resistance is $600\,\Omega$. **8**

    b) Derive the equations used above. **12**

Module – II

13. a) With neat cross-sectional sketch, explain the working of an N-channel depletion mode MOSFET and describe its drain and transfer characteristics. **10**

    b) Draw the CD amplifier using JFET. Deduce its equivalent circuit. Derive equations for its R_i, Av and R_o. **10**

OR

14. Draw the circuit of a single stage RC coupled CE amplifier using equivalent circuits, deduce equations for its

    i) A_v at low, medium and high frequencies

    ii) f_L and

    iii) f_H. **20**

Module – III

15. a) Explain the origin and magnitude of harmonic distortion in power amplifiers. Explain how even harmonics are eliminated in push-pull amplifiers. 8

    b) Draw the circuit of a series pass voltage regulators with feedback. Design it for $V_0 = 6V$, maximum load current of 60 mA. Explain its regulation action (line and load regulation). 12

OR

16. a) Draw an RC phase shift oscillator using BJT with the h-parameter equivalent circuit, derive expression for gain and frequency. 12

    b) Draw a circuit containing voltage shunt feedback and derive its gain, input and output resistances. 8

Module – IV

17. Draw a dual input balanced output emitter coupled differential amplifier. Obtain its equivalent circuit. Derive equations for its differential input resistance A_d, A_c and CMRR. Suggest methods to improve the CMRR. Draw circuits which can give better CMRR and explain. 20

OR

18. a) Draw and design an op-amp circuit to have an output $V_o = 3V_1 - 2V_2 + 5V_3$, where V_1, V_2 and V_3 are analog inputs. 8

    b) Draw a Schmitt trigger using op-amp, for LTP = + 2.5V and UTP = + 5.5 V. Design the circuit. 12

(4×20= 80 Marks)